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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,780	03/23/2004	Susumu Okazaki	1111.70127	2380

7590 10/09/2007

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EXAMINER
A, MINH D

ART UNIT	PAPER NUMBER
2821	

MAIL DATE	DELIVERY MODE
10/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/806,780	OKAZAKI ET AL.	
	Examiner	Art Unit	
	Minh D. A	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 7/6/07.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 3-7,13,15-19,21 and 22 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 3-7,13,15-19 and 21-22 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 13, 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 13, line 3, the phrase " forming on one surface of a first substrate a plurality of light emitting elements " and line 9, the phrase "forming on one surface of a second substrate a circuit " render the claim indefinite because it is unclear whether the limitation(s) following the phrase are part of the claimed invention. See MPEP § 2173.05(d).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 3-7, 13, 15-19 and 21-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Yoshida (Patent No; 6, 7,233, 306).

Regarding claim 3, figures 2-5 and 15, Yoshida discloses that, a display device(100) comprising a first substrate (20) having on one surface thereof: a plurality of light emitting elements (see figure 2) and a thin film transistor matrix (30) for controlling the light emitting elements including a plurality of scan bus lines (3a), a plurality of data bus lines (6a) intersecting the plurality of scan bus lines (3a), and a plurality of thin film transistors (30) arranged respectively at intersections between the plurality of scan bus lines (3a) and the plurality of data bus lines(6a), and electrically connected to the respective plurality of the light emitting elements (see figure 2); and a second substrate (10) having thereon a circuit(201 and 202) for controlling the plurality of the thin film transistors (30), said second substrate(10) being bonded to said one surface of the first substrate(20), and an element (52) for sealing a space where the plurality of the light emitting elements are formed. Col.5, lines 3-67 to col.13, lines 1-65.

Regarding claim 4, figures 2-5 and 15, Yoshida discloses that, wherein a scan bus line control circuit (204) for controlling signals inputted into the plurality of scan bus lines, and a data bus line control circuit (202) for controlling signals outputted from the plurality of data bus lines are formed on the first substrate. Col.5, lines 3-37.

Regarding claim 5, figures 2-5 and 15, Yoshida discloses that, wherein the circuit includes a scan bus line control circuit (204) for controlling signals inputted into the plurality of scan bus lines, and a data bus line control circuit (202) for controlling signals outputted from the plurality of data bus lines.

Regarding claims 6-7, Yoshida discloses that, the second substrate being a printed circuit board. See figures 2 and 15.

Regarding claim 13, figures 2-5 and 15, Yoshida discloses a substrate (20) for forming on one surface of a first substrate a plurality of light emitting elements (see figure 2) and thin film transistor matrix for controlling the light emitting elements including a plurality of scan bus lines (3a), a plurality of data bus lines(6a) intersecting the plurality of scan bus lines (3a), and a plurality of thin film transistors(30) arranged respectively at intersections between the plurality of scan bus lines(3a) and the plurality of data bus lines(6a) and switching elements electrically connected to said respective plurality of light emitting elements; forming on one surface of a second substrate(10), a circuit for controlling the plurality of the thin film transistors(30) which is to be electrically connected to said plurality of the thin film transistors and bonding the first substrate (20) and the second substrate(10) to each other with the one surface of the first substrate(20) and the one surface of the second substrate(10) opposed to each other to electrically connect the circuit to the plurality of switching elements (30). Col.5, lines 3-67 to col.13, lines 1-65.

Regarding claim 15, figures 1-5 and 15, Yoshida discloses a seal (52) for bonding the first substrate (20) and the second substrate(10) to each other, the first substrate(20) and the second substrate (10) are bonded to each other, via a sealing; compound to seal a space where said plurality of light emitting elements are formed wherein a gas is sealed within said space.

Regarding claims 16-17, figures 1-5 and 15, Yoshida discloses that, the light emitting elements are organic EL elements and the first substrate and the second

substrate are electrically connected to each other by columnar electrodes formed between the first substrate and the second substrate.

Regarding claims 18-19, figures 1-5, and 15, Yoshida discloses that, the first substrate and the second substrate are electrically connected to each other by a flexible substrate and a light emitted by the light emitting elements is taken out toward the other surface of the first substrate and a sealing compound for sealing a gas within said space defined between said first substrate and said second substrate.

Regarding claims 21-22, figures 1-5 and15, Yoshida discloses that, a sealing compound for sealing a gas within said space defined between said first substrate and said second substrate and the light emitting element and the switching element are positioned so as to overlap in a normal direction of the first substrate and the second substrate.

Response to Arguments

5. Applicant's arguments with respect to claims 3-7, 13, 15-19 and 21-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Citation of relevant prior art

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Isami et al (US 6,791,521) and Yamazaki et al. (US 6,563,482) are cited to show a display device.

Inquiry

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Dieu A whose telephone number is (571) 272-1817. The examiner can normally be reached on M-F (5:30 AM-2: 45 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Owens Douglas W can be reached on (571) 272-1662. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Examiner

Minh A

Art Unit 2821

9/19/07

Shih-Chao Chen

SHIH-CHAO CHEN
PRIMARY EXAMINER